1 (Once Amended). A system comprising:

a processor; and

a memory device operatively coupled to the processor, the memory device comprising a plurality of vertically stacked ball grid arrays, each ball grid array having a memory chip, and wherein the vertically stacked ball grid arrays comprise:

a plurality of packages, each of the plurality of packages comprising a plurality of mateable alignment features, and wherein each of the plurality of packages is physically coupled to another of the plurality of packages; and

a plurality of memory chips, each of the plurality of memory chips physically coupled to a respective one of the plurality of packages.

3 (Once Amended). The system, as set forth in claim 1, wherein each package comprises:

a molded resin body having a die side and a wire side.

4 (Once Amended). The system, as set forth in claim 3, wherein each package comprises:

a plurality of first mateable alignment features on the die side of the package; and

a plurality of second mateable alignment features on the wire side of the package.

5 (Once Amended). The system, as set forth in claim 4, wherein the plurality of first mateable alignment features are male and the plurality of second mateable alignment features are female.

6 (Once Amended). The system, as set forth in claim 4, wherein the plurality of first mateable alignment features are male and the plurality of second mateable alignment features are male.

7 (Once Amended). The system, as set forth in claim 4, wherein the plurality of first mateable alignment features are female and the plurality of second mateable alignment features are male.

8 (Once Amended). The system, as set forth in claim 4, wherein the plurality of first mateable alignment features are female and the plurality of second mateable alignment features are female.

9 (Once Amended). The package, as set forth in claim 4, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features orient adjacent packages in a unique location.

10 (Once Amended). The package, as set forth in claim 9, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features are arranged asymmetrically.

A2 cancld

11 (Once Amended). The package, as set forth in claim 9, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features comprising of at least one unique alignment feature.

12 (Once Amended). The package, as set forth in claim 4, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features support adjacent packages during solder ball reflow.

13 (Once Amended). The system, as set forth in claim 1, wherein each of the plurality of packages is electrically coupled to another of the plurality of packages using solder balls.

15 (Once Amended). A memory board comprising:

a substrate; and

a memory device operatively coupled to the substrate, the memory device comprising a plurality of vertically stacked ball grid arrays, each ball grid array having a memory chip, and wherein the vertically stacked ball grid arrays comprise:

a plurality of packages, each of the plurality of packages comprising a plurality of mateable alignment features, and wherein each of the plurality of packages is physically coupled to another of the plurality of packages; and

a plurality of memory chips, each of the plurality of memory chips coupled to a respective one of the plurality of packages.

19 (Once Amended). The memory board, as set forth in claim 15, wherein the package comprises:

a molded resin body having a die side and a wire side.

20 (Once Amended). The memory board, as set forth in claim 19, wherein the molded resin package comprises:

a plurality of first mateable alignment features on the die side of the package; and

a plurality of second mateable alignment features on the wire side of the package.

21 (Once Amended). The memory board, as set forth in claim 20, wherein the plurality of first mateable alignment features are male and the plurality of second mateable alignment features are female.

A4 cont.

22 (Once Amended). The memory board, as set forth in claim 20, wherein the plurality of first mateable alignment features are male and the plurality of second mateable alignment features are male.

23 (Once Amended). The memory board, as set forth in claim 20, wherein the plurality of first mateable alignment features are female and the plurality of second mateable alignment features are male.

24 (Once Amended). The memory board, as set forth in claim 20, wherein the plurality of first mateable alignment features are female and the plurality of second mateable alignment features are female.

25 (Once Amended). The package, as set forth in claim 20, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features orient adjacent packages in a unique location.

26 (Once Amended). The package, as set forth in claim 25, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features are arranged asymmetrically.

27 (Once Amended). The package, as set forth in claim 25, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features comprising of at least one unique alignment feature.

28 (Once Amended). The package, as set forth in claim 20, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features support adjacent packages during solder ball reflow.

29 (Once Amended). The memory board, as set forth in claim 15, wherein each of the plurality of packages is electrically coupled to another of the plurality of packages using solder balls.

33 (Once Amended). A stacked ball grid array comprising:

a plurality of packages, each of the plurality of packages comprising a plurality of mateable alignment features, and each of the plurality of packages coupled to another of the plurality of packages; and

a plurality of memory chips, each of the plurality of memory chips coupled to a respective one of the plurality of packages.

35 (Once Amended). The stacked ball grid array, as set forth in claim 33, wherein the package comprises:

a molded resin body having a die side and a wire side.

36 (Once Amended). The stacked ball grid array, as set forth in claim 35, wherein the molded resin package comprises:

a plurality of first mateable alignment features on the die side of the package; and

a plurality of second mateable alignment features on the wire side of the package.

37 (Once Amended). The stacked ball grid array, as set forth in claim 36, wherein the plurality of first mateable alignment features are male and the plurality of second mateable alignment features are female.

A6 cont

38 (Once Amended). The stacked ball grid array, as set forth in claim 36, wherein the plurality of first mateable alignment features are male and the plurality of second mateable alignment features are male.

39 (Once Amended). The stacked ball grid array, as set forth in claim 36, wherein the plurality of first mateable alignment features are female and the plurality of second mateable alignment features are male.

40 (Once Amended). The stacked ball grid array, as set forth in claim 36, wherein the plurality of first mateable alignment features are female and the plurality of second mateable alignment features are female.

41 (Once Amended). The package, as set forth in claim 36, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features orient adjacent packages in a unique location.

42 (Once Amended). The package, as set forth in claim 41, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features are arranged asymmetrically.

43 (Once Amended). The package, as set forth in claim 41, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features comprising of at least one unique alignment feature.

44 (Once Amended). The package, as set forth in claim 36, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features support adjacent packages during solder ball reflow.

45 (Once Amended). The stacked ball grid array, as set forth in claim 33, wherein each of the plurality of packages is electrically coupled to another of the plurality of packages using solder balls.

47 (Once Amended). A device comprising:

a chip; and

a package operatively coupled to the chip, the package comprising:

a first side;

a second side;

a plurality of first mateable alignment features on the first side of the package; and

a plurality of second mateable alignment features on the second side of the package.

49 (Once Amended). The device, as set forth in claim 47, wherein the plurality of first mateable alignment features are male and the plurality of second mateable alignment features are female.

50 (Once Amended). The device, as set forth in claim 47, wherein the plurality of first mateable alignment features are male and the plurality of second mateable alignment features are male.

A8 cont'd

51 (Once Amended). The device, as set forth in claim 47, wherein the plurality of first mateable alignment features are female and the plurality of second mateable alignment features are male.

52 (Once Amended). The device, as set forth in claim 47, wherein the plurality of first mateable alignment features are female and the plurality of second mateable alignment features are female.

C1

54 (Once Amended). A package comprising:

A9

a first side;

a second side;

a plurality of first mateable alignment features on the first side of the package; and

a plurality of second mateable alignment features on the second side of the package.

56 (Once Amended). The package, as set forth in claim 54, wherein the plurality of first mateable alignment features are male and the plurality of second mateable alignment features are female.

57 (Once Amended). The package, as set forth in claim 54, wherein the plurality of first mateable alignment features are male and the plurality of second mateable alignment features are male.

A10

58 (Once Amended). The package, as set forth in claim 54, wherein the plurality of first mateable alignment features are female and the plurality of second mateable alignment features are male.

59 (Once Amended). The package, as set forth in claim 54, wherein the plurality of first mateable alignment features are female and the plurality of second mateable alignment features are female.

60 (Once Amended). The package, as set forth in claim 54, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features orient adjacent packages in a unique location.

61 (Once Amended). The package, as set forth in claim 60, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features are arranged asymmetrically.

62 (Once Amended). The package, as set forth in claim 60, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features comprising of at least one unique alignment feature.

63 (Once Amended). The package, as set forth in claim 54, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features support adjacent packages during solder ball reflow.